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Reducing EMI and Improving Signal Integrity Using Spread Spectrum Clocking

Electromagnetic interference (EMI), once the exclusive concern of equipment designers working with high-speed signals, is no longer limited to a narrow class of high-end applications. Continued innovation in semiconductor technology has resulted in the ready availability of cost-effective, high-performance system-on-chip (SoC) devices, microcontrollers (MCUs), processors, digital signal processors (DSPs), application-specific integrated circuits (ASICs), field-programmable gate arrays (FPGAs) and analog/digital converters (ADCs). The high-speed clocking signals required to drive these ICs, however, generate more EMI and, as a consequence, more challenges for designers of consumer, enterprise, communications and embedded equipment.

Unfortunately, EMI problems are not limited to clocks. Buses, interconnects and networking interfaces also employ data rates and high-speed signals that can generate unwanted EMI. EMI is also becoming an issue with digital power supplies, which increase their efficiency by using higher switching frequencies. The situation grows worse with every new product generation given the combination of steady increases in clock speeds and decreases in supply voltages that reduce overall noise margins. If left unattended, these high frequency signals and their harmonics (see Figure 1) can have peak energy levels that exceed FCC Class A and Class B Part 15 EMI limits and delay products from being released to market. These issues, coupled with shorter design cycles, increasing sensitivity to cost imposed by high-volume markets and shorter product life spans, make it challenging for developers to produce quality products in a timely fashion.

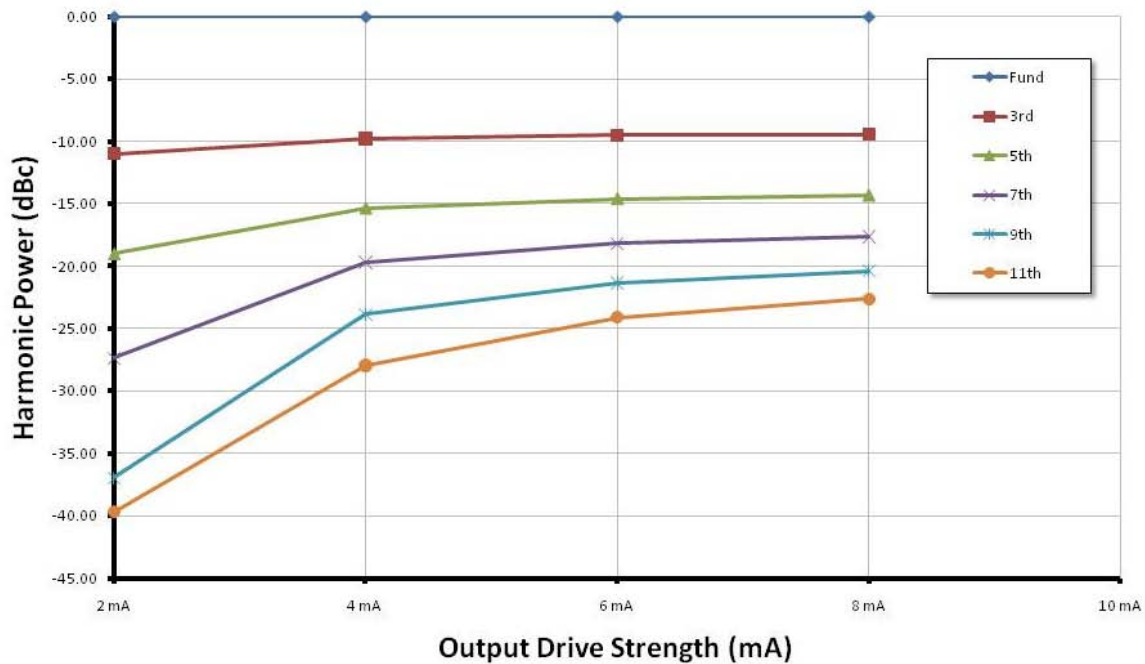


Figure 1. Si5350/51 Relative Carrier and Harmonic Power vs. Output Drive Strength at 10 MHz

Electromagnetic Interference (EMI)

Any charge moving in an electrical field or change in field emits electromagnetic radiation, with the strength of the radiation being directly proportional to the rate and size of change. Sometimes electromagnetic emissions are intentional, such as when transmitting data through a cellular phone antenna, but many digital systems, such as PCs, PDAs, smartphones, printers and scanners, emit unintentional radiation that can interfere with nearby circuits. Within these systems, periodic clock signals are a major cause of EMI radiation.

Fundamental and odd multiples of fundamental sinusoidal frequencies (i.e., harmonics) make up a square wave. Harmonic frequencies set the exact frequency of the radiation spectrum while drive levels set the bandwidth or radiation strength of each harmonic. As a consequence, EMI radiation increases with higher edge speeds (rise and fall times) and higher drive levels.

Shielding is a well-known method of preventing EMI emissions by containing them within the system and fully or partially covering the emission locations with grounded conductive shields. Shielding can be an effective approach in systems with strong emissions. However, for many systems, especially portable and handheld products, shielding is perhaps the least desirable method for reducing EMI emissions. Shielding not only increases the size, weight and cost of a system (factors that cannot be compromised in many applications), but it also substantially increases labor costs.

Another widely used technique for reducing existing EMI emissions generated by clocks and timing signals is to use low-pass filters to eliminate high-order harmonics. Specifically, this approach reduces the rise and fall times of a signal and, consequently, the radiated EMI. This technique, however, is often not viable for high-speed systems since reducing rise and fall times through filtering also reduces critical setup-and-hold-time margins, increases the amount of signal overshoot, undershoot and ringing, and increases the susceptibility of the clock to other interferers, all of which impact the jitter performance.

Another major issue with filtering is that it is not systemic and only produces a limited, local effect. This means that even though emissions have been reduced for a given node in the system, it is not reduced in other nodes. Consequently, the overall reduction in emissions may be marginal. A better technique is required to address all sources of EMI.

Spread Spectrum Clocking

Although the fundamental causes of EMI are relatively straightforward, accurately simulating the entire system is difficult, time-consuming and error-prone due to the use of hard-to-predict models and complex parameter extractions. Rather than attempt to tune existing EMI levels to within acceptable limits, the most effective strategy for ensuring compliance is to employ design techniques that reduce the introduction of EMI in the first place. In addition, eliminating EMI at its source means greater signal integrity throughout the system, not just where local filters have been placed.

One of the most effective and efficient approaches to controlling and reducing EMI is to use spread spectrum clock generation (SSCG) technology. Instead of maintaining a constant frequency, spread spectrum techniques modulate the system clock across a much smaller frequency that creates a frequency spectrum with sideband harmonics. By intentionally spreading the narrowband repetitive clock across a broader band, the peak spectral energy of both the fundamental and harmonic frequencies can be reduced simultaneously (see Figure 2). The modulation frequency (FM) is typically 30 to 33 kHz, which is broad enough to spread the energy around the carrier yet narrow enough to avoid creating timing and tracking issues in the system.

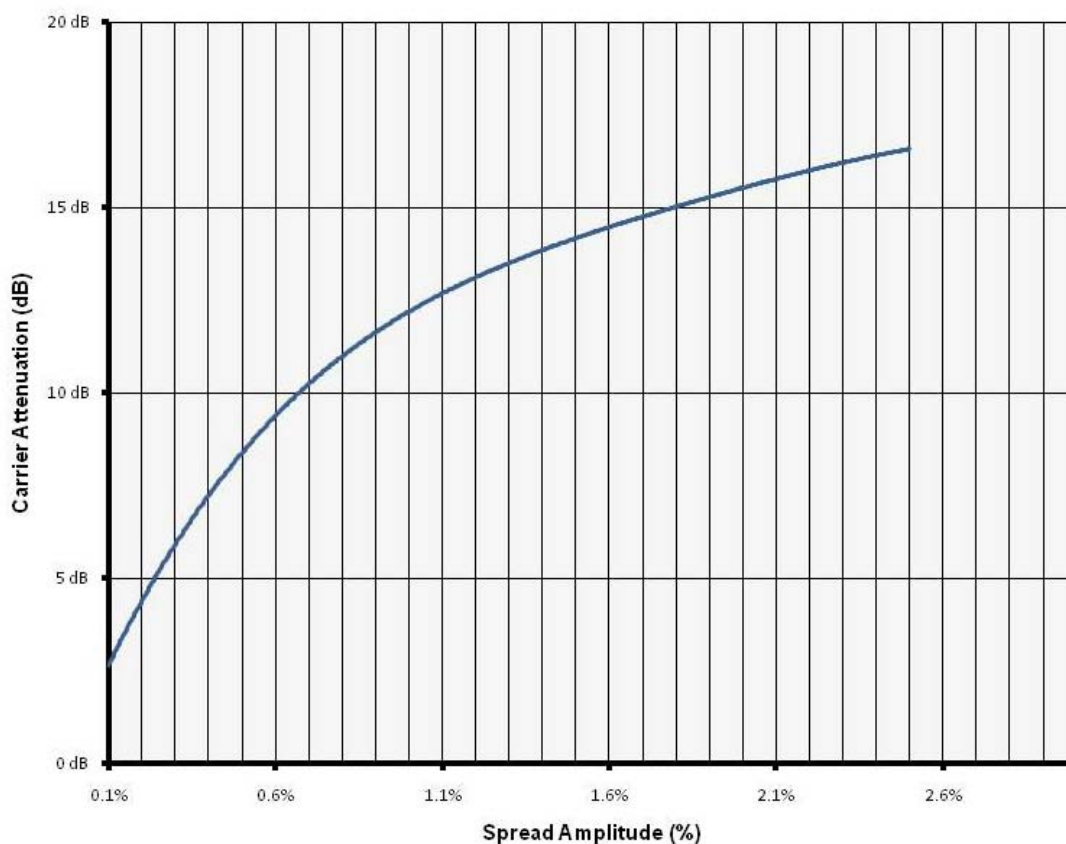


Figure 2. SSCG Reduces EMI at any Single Frequency

Effectively, an SSCG clock IC adds controlled jitter by linearly increasing and decreasing the clock frequency. While the total radiated energy in the signal is the same as an unmodulated signal, the spectral components occur at a much lower magnitude because it is spread across more frequencies/greater bandwidth. Thus, and developers are able to reduce EMI to desired levels. In addition, by keeping the frequency spread small, SSCG technology reduces EMI without degrading signal timing quality as measured by period and cycle-to-cycle jitter (see Figure 3).

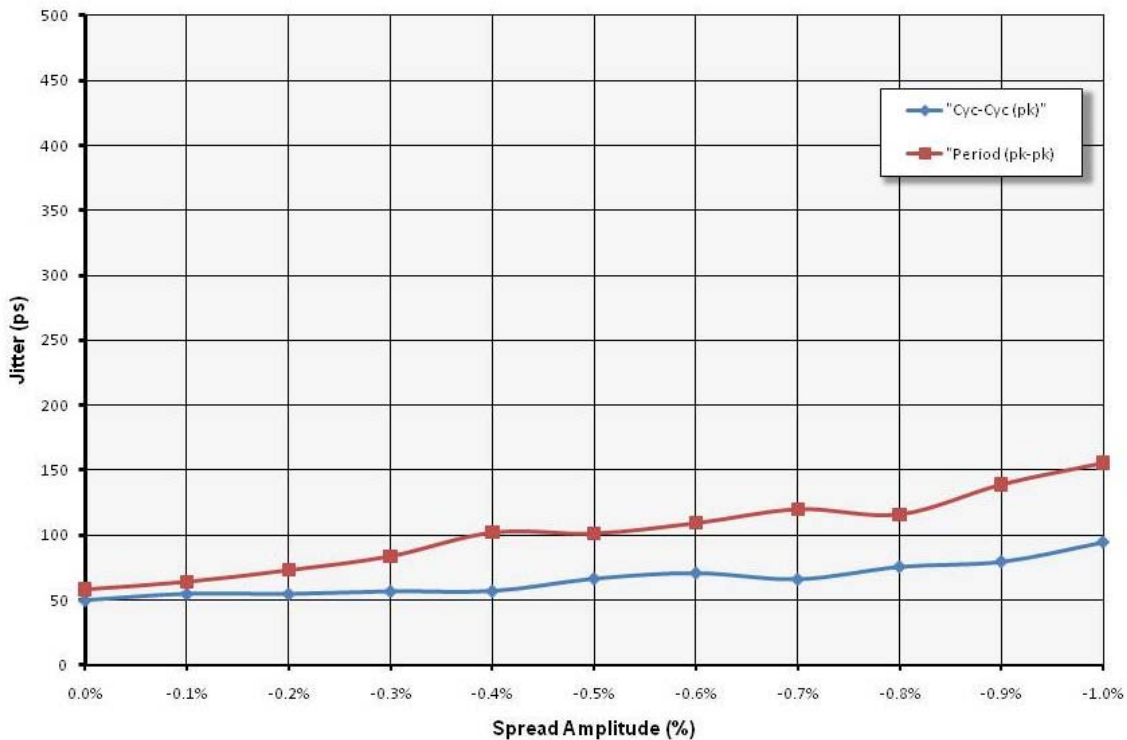


Figure 3. SSCG Minimizes Period and Cycle-to-Cycle Jitter

Consider a 32 kHz, nonlinear frequency profile modulating a 66.666 MHz system clock. Because the modulation is centered on the system clock frequency (in this case, 66.666 MHz), this type of profile is known as center spread frequency modulation. The amount of relative EMI reduction on the same clock using $\pm 1.5\%$ frequency modulation limits compared to an unmodulated system clock are shown for the fundamental frequency and third-order harmonics. Altering the profile changes how EMI is spread. For example, the relative EMI reductions for the same 66.666 MHz clock and $\pm 1.5\%$ center spread using a triangular profile are different for the fundamental frequency and third-order harmonics.

Spread-spectrum clock generation results in a dramatic reduction of EMI throughout the system compared to other EMI-reduction methods. Specifically, since all clock and timing signals derived from an SSCG clock are modulated by the same percentage (including buses and interconnects), EMI reductions from SSCG technology benefit the entire system, not just a local circuit. For many applications, implementing a spread spectrum clock into a system during the early design stages can completely mitigate the need for further EMI reduction measures.

Programmable Spreading

Tuning a fixed-function clock generator for a system often requires matching analog components. Rather than having to swap out different analog components to optimally match a system and reduce EMI, programmable clock generators support customization through simple configurable clock parameters that optimize the clock output to match the required application performance (see Table 1). This approach simplifies development by eliminating the complex calculations involved in manually tuning a system. Programmable clock devices also enable developers to reduce design risks by easily and quickly accommodating late design changes that impact timing parameters.

Table 1. Silicon Labs SL15100 SSCG Programmable Clock Parameters

Programmable Parameter	Range	Resolution
Output-to-Output Skew	-160 to +160 psec	20 psec
Output Drive Strength	20 to 100 $\square$	20 $\square$
Output Rise/Fall Times (15 pF Clock)	0.3 to 4.2 psec	0.3 nsec
Duty Cycle	-3% to +3%	1%
Frequency	1 to 200 MHz	2 ppm
Spread Spectrum Amplitude	0% to 5%	0.05%
Spread Spectrum Modulation	16 to 128 kHz	1 kHz

One of the most critical considerations for clock-signal integrity is matching board trace and driven load impedance to the clock driver. This matching ensures that the clock signal is free from overshooting or undershooting and ringing for each of the driven clock signals. Programmable clocks achieve this goal by providing adjustable impedance levels at each clock-output driver to ensure an optimal match to various load-impedance levels. Programmable clock drive strength levels allow developers to match load-impedance levels individually for each output, obtain matched impedance levels, and optimize signal integrity based on the actual levels measured during system evaluation. In addition, programmable drive levels can be used to control the clock signal rise and fall times within acceptable signal integrity limitations to slow the edges. This further reduces radiated EMI by decreasing the total high-frequency harmonic content of the signal.

The flexible frequency modulation of programmable clocks also simplifies electromagnetic compatibility (EMC) testing. Because the frequency modulation can be varied (for example, frequency modulation can vary from 0% to 5% with the Silicon Labs SL15100 SSCG clock IC), it is much easier to make compatibility measurements during design and testing. The ability to take this feedback into early design stages eliminates the need for costly late-design modifications, avoids production introduction delays and can substantially improve time-to-market.

Developers of systems where emissions are within acceptable limits and products meet EMC requirements may also benefit from the use of spread spectrum clock generators. For example, many high-volume consumer products, such as ink-jet/multifunction printers or PDAs, use multiple board layers to increase signal margin. By using an SSCG clock in such designs, it is often possible to reduce emission levels even further, enabling the system to be implemented with fewer board layers and resulting in substantial cost savings.

Timing Options

System developers can choose from a wide variety of general-purpose, low-voltage CMOS clock ICs optimized for EMI reduction. For example, Silicon Labs' Si5350/51 clock IC (see Figure 4) provides a programmable solution with up to eight outputs at frequencies up to 150 MHz for high-volume, cost-sensitive applications, such as digital cameras, printers, graphics cards, set-top boxes, HDTVs and home gateways. These clock devices typically operate at low power (26 mW core power) and require less board space (4.0 mm x 4.0 mm package size) compared to other clocking technologies and support individual control of SSC (i.e., on/off) for each output frequency.

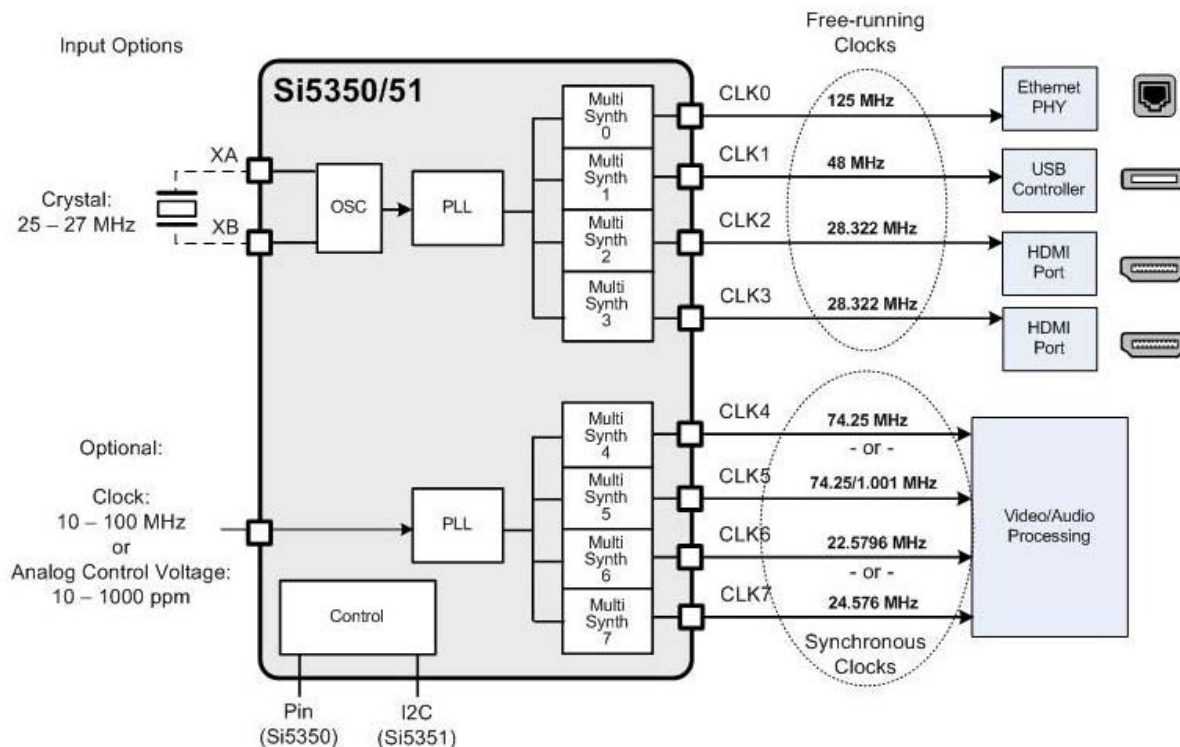


Figure 4. Si5350/51 Programmable General Purpose Clock IC

Clock generators optimized for specific interconnect standards, such as PCI Express clock ICs, are also available. Available as both fixed-function and factory-customizable clocks, these devices comply with PCI Express Gen 1, Gen 2 and Gen 3 for use in a wide array of consumer, server, storage, medical and test equipment applications. PCI Express clocks also support SSC as specified in the PCI Express standards.

Processor-specific clock generators are also available to developers. For example, x86 drop-in replacement clocks provide low-power operation for x86-based embedded applications, such as storage, blade server, set-top box, medical, test equipment and home and industrial automation applications. Because they have been optimized for x86-based applications, they offer integrated features that eliminate the need for many board-level components, such as external resistors and level translators, and result in lower system cost.

Developers should also be aware of clock distribution devices available to reduce EMI while distributing clock signals throughout a system. These clock distribution devices are capable of tracking the spread spectrum and can pass it through the distributed clocks. Devices, such as zero-delay LVCMOS and PCI Express fanout buffers, are designed for use in servers, routers and switches, while temperature-controlled XO (TCXO) fanout buffers are excellent solutions for smart phones, tablets and other portable systems.

Note that many EMI reduction and timing features can be integrated into an SSCG device to achieve higher performance. Some clocks support multiple outputs, and many are available with multiple PLLs with selective use of spread spectrum clock functions to enable developers to integrate key components, such as buffers and level translators. For example, Silicon Labs' SL15100 clock IC with an integrated PLL clock multiplier, built-in frequency dividers and switch circuits provides two outputs, while the SL28PCIe30 device has more functionality and up to nine outputs. The availability of multiple output clocks based on a first-order crystal (each with its own range of programmable values) eliminates the need for a larger number of crystals and crystal oscillators, resulting in significant BOM cost savings and smaller board size. For portable devices, the use of programmable SSCG clock ICs improves power consumption compared to traditional clocking topologies designed to extend battery life.

For high-volume applications, developers also have the option of creating custom-configuration clocking devices to optimize jitter performance, functionality and cost. For example, to help accelerate the design process, Silicon Labs offers the Web-based ClockBuilder utility (www.silabs.com/ClockBuilder), which streamlines clock product selection and device configuration and enables specification of custom timing devices for a variety of applications with or without SSC.

Summary

Evaluating and simulating radiated EMI can be an extremely complex process. By employing simple adjustments in layout, adjusting rise/fall times, and using spread spectrum clocking technology, developers can sufficiently reduce radiated power for many applications without the need for complex analysis or simulations.

SSCG clock ICs provide a cost-effective approach to managing EMI by eliminating EMI at its source. With their high level of integration and flexible timing parameters, SSCG devices simplify system design and eliminate the need for many expensive discrete components while improving performance, minimizing board space and reducing time-to-market.